Amendments to the Specification:

Please replace the paragraph beginning at page 6, line 23, with the following amended paragraph:

Referring to the block diagram of FIG. 2, where like reference numerals refer to like entities, a more detailed explanation of the receiver 111 and communications signal processor 113 will be undertaken. The receiver 111 includes a down converter or mixer 201 for translating the radio frequency signal to a lower or intermediate frequency signal. This lower frequency signal after suitable amplification is applied to a frequency discriminator 205 which converts the frequency variations of the applied signal to an analog base band signal. This analog signal is filtered in a low pass post detection filter (PDF) 207 to remove high frequency components created by or magnified by the discriminator 205. The output of the PDF 207 is applied to an analog to digital converter (A/D) 209 that in the preferred form provides 4 samples, each of 4 or more bits, for each symbol period or 4 million samples per second at the output 211. These samples are coupled to the communications signal processor 113 ~~213~~. The balance of FIG. 2 duplicates the above discussions of FIG. 1.

Please replace the paragraph beginning at page 7, line 6, with the following amended paragraph:

Referring to FIG. 3 a more detailed block diagram for the receive portion of the communications signal processor 113 will be reviewed. The sample stream from the A/D is applied to a detector 301. Detector 301 processes the samples corresponding to a sync pattern, preferably the first 72 symbols to determine whether an access code, essentially the address of the communications unit, is present. When the access code is detected the switch 302 is closed and the samples, as processed (re-sampled) by the detector, are routed from the detector 301 to a signal processor 304. If the access code is detected the detector 301 further determines timing and carrier synchronization. This provides an initial carrier estimation f_{co}, and timing estimation, specifically CLK and FRAC for the first symbol to be recovered. CLK is the sample index of the incoming samples and FRAC is a fraction of a sample. The particulars of the detector 301 can be found in co-pending application SN 09/709690, now U.S. Patent No. 6,424,673, by Chen et al., filed on November 10, 2000 and titled METHOD AND APPARATUS IN A WIRELESS COMMUNICATION SYSTEM FOR FACILITATING DETECTION OF, AND SYNCHRONIZATION WITH, A PREDETERMINED SYNCHRONIZATION SIGNAL, assigned to the same assignee as here and hereby incorporated herein in its entirety. For various performance motivated reasons the preferred receiver architecture including the communications signal processor and more specifically the signal processor was chosen to be a maximum likelihood sequence estimator (MLSE). This is discussed in co-pending application SN 09/794285, by Chen filed on February 27, 2001 and titled APPARATUS FOR RECEIVING

AND RECOVERING FREQUENCY SHIFT KEYED SYMBOLS, assigned to the same assignee as here and hereby incorporated herein in its entirety.

Please replace the paragraph beginning at page 7, line 30, with the following amended paragraph:

This disclosure will focus more on the inventive principles and concepts or specifics of the operation and function and preferred embodiment of this signal processor or an embodiment of a portion of this architecture. As a quick overview the samples of the received signal are coupled to the signal processor 304 that includes a frequency and phase or timing adjustment function 303 coupled to a correlator 305 that is coupled to a trellis processor 307 and then to a symbol selector 309. Lastly a carrier tracking function 313 is coupled to the detector 301, correlator 305, and the output of the symbol selector 309 and provides a carrier adjustment input to the adjustment function 303. The adjustment function ~~provide~~ provides adjusted samples to the correlator 305. The correlator performs a correlation between 4 samples of the received signal and a plurality of templates, each comprised of 4 predetermined values, where the templates each correspond to what would be the expected received signal samples for each possible symbol or symbol state transition. These correlations are provided to the trellis processor 307. The trellis processor determines or calculates a metric or weight for a path corresponding to each possible branch from each symbol state to all others for each symbol period and selects the better path including corresponding branch that terminates at each symbol

state. These paths and respective relative weights are provided to the symbol selector 309. The symbol selector selects a symbol for a given symbol period n to be the symbol corresponding to the better path metric at a later symbol period n+l, where l = 2 in the preferred embodiment. These symbols are coupled to a decoder 311 operating in known fashion and according to the Bluetooth standards in the preferred embodiment for decoding the particular symbols. The decoder 311 will not be further discussed herein, however, the operation and function of each of the other entities will be explained in more detail below with reference to FIG. 4. However it is advisable to first explain the symbol transition diagram 500 of FIG. 5.